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Evolution of Processors and its Implication in Data Computation Capability

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Summary

New techniques in seismic data processing and geophysical simulations require more and more huge amount of computing power. The new and innovative algorithms developed by research community hardly may run on the existing computing systems of the companies. Cluster system; grid/cloud computing has evolved to run these high computing algorithms. But maintaining these systems their networking problems comes at a price to the companies. Hence, there is urgent need of high computing processors which are the heart of the servers, workstations to be utilized in the industry. In this paper the historical development of the processors are discussed in brief and analyzed that how the increasing computing power of processors had reflected in the seismic industry to run higher computing algorithms. Still more is expected from the IT industry to solve the computational requirement of Petroleum industry. Due to introduction of new techniques like processing of data acquired by Broadband data acquisition techniques, 3D multiple attenuation Reverse time migration, Full wave inversion industry is not satisfied with the present computing capabilities.

Keywords: *Computer Processor, Microprocessor, Computing Power*

Introduction

Like evolution of human, from ape to well developed, educated, gentleman; computer processors also have gone through enormous changes during its journey from 1971 till 2013 and it is expected that the advancement in this field will shoot like rocket in coming future. Servers, workstations etc. are used in Seismic Data Processing. While designing any processors some things which are always focused on – a) Small Size b) High Speed c) Better Performance and efficiency c) Low Power consumption in turn low heat dissipation. Overall Seismic data processing is highly CPU (Central Processing Unit) and GPU (Graphics Processing Unit) intensive job. Till some time back processors used to come in separate to the Graphics Processing Unit. Now a days both are integrated in the same die. In comparison to the earlier processors which were of single physical core with less clock speed, with less bus bandwidth, high latency etc., recent processors are of multi core with multi threads (up to 8 core/16 threads) with high clock rate and very less latency. Induction of new technology like Turbo Boost(in which processor runs with higher clock frequency when requested by the operating system to meet the performance requirement), Hyper threading (this technology is introduced by Intel to use parallel computation, in which operating system address two virtual core for each physical core), Quick Path interface (this is also introduced by Intel, in which two processor interact with each other in order to share the load), has strengthen the computing systems.

Due to this technology advancement the time taken for a particular seismic data processing job has reduced significantly and in turn reduced the production cost, with better results, which is our prime objective.

Evolution of Processors

Evolution of Processors: Table 1 shows the basic Comparison of processor in chronological order:

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Years	1971	1972
Bit	4 bit	8 bit
Clock Speed	2 MHz	5 MHz
No. of Core	Single core	Single core
Manufacturing Technology	6 µm	3 µm
No of transistors	4,500	29,000
		
	INS4004	C8008

1978	1986	2006
16 bits	32 bit	64 bit
66 MHz	500 MHz	2.93 GHz
Single core	Single core	Dual Core
0.8 µm	0.18 µm	65 nm
31,00,000	95,00,000	291,000,000
		
D8086	Intel i376	Itanium

2009	**2011**	**2013**
64 bit	**64 bit**	**64 bit**
2.7 GHz Turbo 3.3 GHz	**3.7 GHz Turbo 4.1 GHz**	**3.6 GHz Turbo 4.0 GHz**
Multi core(2,4,6,8)	**Multi core(2,4), Higher core yet to release**	**Multi core(2,4) Higher core yet to release**
32 nm	**22 nm**	**22 nm**
42 millions	**731 million**	**1.4 billion**
		

Table 1

Technology transformation of processors is clear from the table, the processors changes from 4 bit to 64 bit, from 2 MHz to 3.6 GHz with Turbo 4.0GHz, from single physical core to multi core (2,4,6,8) and 10 core and 12 core processors are in pipeline and above all the manufacturing technology is changed from 6µm to 22 nm.

Current status

In this paper, current and its successor processor technology is discussed in detail.

i) Sandy Bridge Processor:

Sandy Bridge is the codename of the microarchitecture of processor developed by Intel. Intel demonstrated its first sandy bridge processors in 2009 and released in 2011 to replace its older processor named Nehalem. While Nehalem was based on 45 nm manufacturing technology, Sandy bridge processors is based on 32 nm technology and it uses planar double gate transistors. By saying 32 nm, it means half the distance between memory cells.

Planar Double gate transistors:

Planar double-gate transistor is a traditional transistor in which the channel is sandwiched between two independent fabricated gates. Fig 1 shows the schematic diagram of a Planar Double Gate Transistor.

It provides better electrical control over the channel. Due to which leakage current can be reduced. Also, the on state current i.e. drive current is enhances. Due to these advantages power consumption is reduced and performance is enhanced.

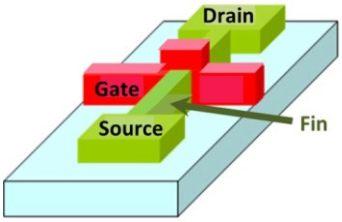

Fig 1-Planar Double Gate Transistor

Features of Sandy Bridge Processors :

- 32 kB data + 32 kB instruction L1 cache (3 clocks) and 256 kB L2 cache (8 clocks) per core
- Sandy Bridge and Graphics has been integrated in the same die and both share L3 cache
- 64-byte cache line size
- Two load/store operations per CPU cycle for each memory channel
- It supports memory speed up to 1333 MHz DDR3 Memory.
- 256-bit/cycle ring bus interconnects between cores, graphics, cache and System Agent Domain.

- Advanced Vector Extensions(AVX) 256-bit instruction set with wider vectors, new extensible syntax and rich functionality
- Up to 8 physical cores or 16 logical cores through Hyper-threading

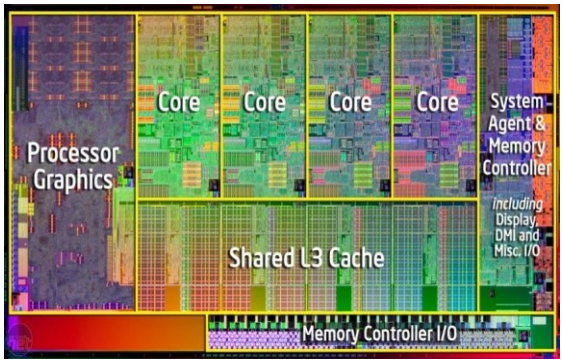

Fig 2-Sandy Bridge die map(32nm, 216 sq mm)

Tick Tock development model of Sandy Bridge:

This model adopted by Intel in which they first release the initial version and later they release the revised version. Tick is shrinkage of process technology and Tock in a new micro architecture. So Sandy Bridge is at tock that means new micro architecture.

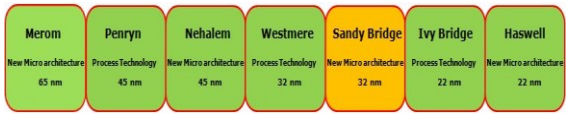

Fig 3:- Development Model of Sandy Bridge

Sandy Bridge Processor and Graphics Integration:

In contrast to its predecessor, Sandy Bridge has integrated Graphics and memory controller with processor on the same die inside the processor package.L3 cache is shared by both processor and GPU. The sharing of cache is configurable. This integration reduces memory latency even more and the overall power efficiency (CPU+ Graphics) is improved.

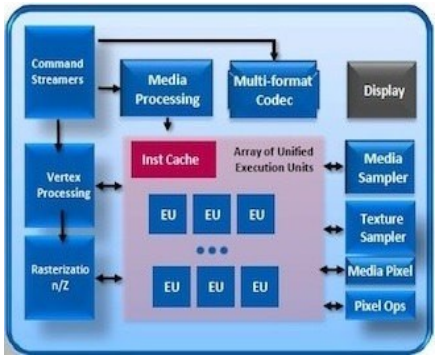

Fig 4- Processor & Graphics integration

ii) Ivy Bridge Processors:

These processors are released in end of 2011. It is third generation Intel core processors. The major changes with respect to the Sandy Bridge processor is a) reduced size with 22 nm manufacturing process b) New random number generator and RdRand. Unlike sandy bridge processor Ivy bridge processors uses tri-gate (3D) transistors. Due to induction of tri-gate transistors, power consumption is reduced by 50% at the same performance level of sandy bridge processors which is very important in case of imbedded systems and mobiles.

Tri-gate (3D) Transistors

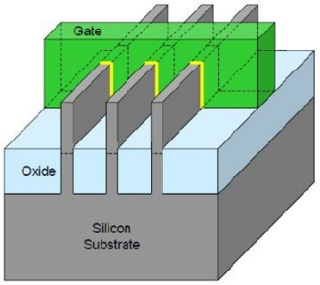

Fig 5:-Tri-Gate (3D) Transistor

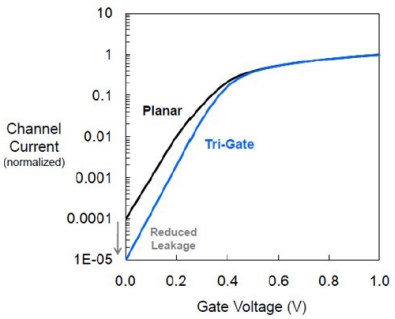

Fig 6:-3D- Gate Transistor Response

In this type of transistors multiple channels is created by using several fins with a single gate. Due to this leakage current is reduced and require much less power than planer transistors. By this technology improves speed by 37% and reduced power consumption by 50 % in comparison to the previous transistors.

Tick Tock development model of Ivy Bridge:

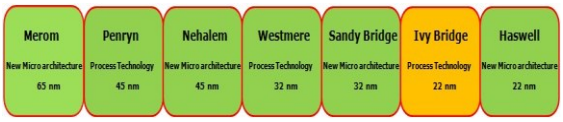

Fig 7:- Development Model of Ivy Bridge

As Ivy Bridge has 22 nm technology ie shrinkage from the previous microarchitecture so Tick.

Significant changes over Sandy Bridge:

- It uses F16C(16-bit Floating-Point conversion instructions)
- Ivy processors support PCI Express 3.0 which was not on Core i3 and ULV processors).
- In Ivy processor Max CPU multipliers 63 in comparison to 57 for Sandy Bridge.
- RAM support up to 2800 MT/s in 200 MHz increments.
- The built-in GPU has 6 or 16 execution units (EUs), compared to 6 or 12 nos. in case of Sandy Bridge.

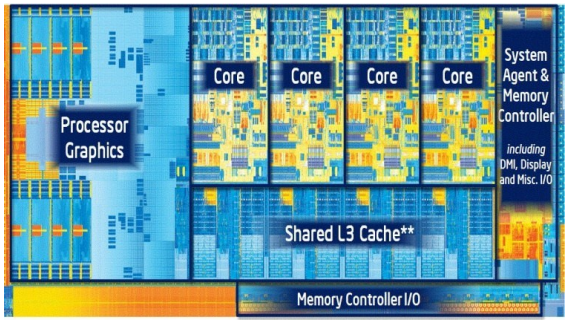

Fig 8:-Ivy Bridge die map (22nm,160 sq mm)

Haswell Processor:

It is the code name of the processor micro architecture with 22 nm manufacturing process. It is the successor of Ivy Bridge (22 nm). It is release recently in the month of June 2013. Haswell is specially designed in order to reduce the power consumption and improve the performance with the help of multi-gate transistor. In server environment four core (8 threads) Haswell processor is available.

Tick Tock development of Haswell

Fig 9:- Development Model of Haswell

There is some significant changes like additional one no of Arithmetic Logic Unit, one no of Graphics Logic Unit in each core, one no of Branch Prediction Unit, Deeper Buffer and high cache bandwidth. Due to the above changes following improvement is seen in comparison to Ivy Bridge Processors:

- Haswell has approximately 8% better vector processing performance.
- It has up to 6% faster single-threaded performance.
- 6% faster multi-threaded performance.
- Haswell draws around 8% more power under load than Ivy Bridge.
- A 6% increase in sequential CPU performance (eight execution ports per core versus six).
- Up to 20% performance increase over the integrated Graphics Processing Unit
- Total performance improvement on average is about 3%.

Implication of development in processors in Seismic Data Processing

The complexity of processing application software is increasing consistently which include more complex operation on data set. Hence the processors are on real test in terms of their computing capability.

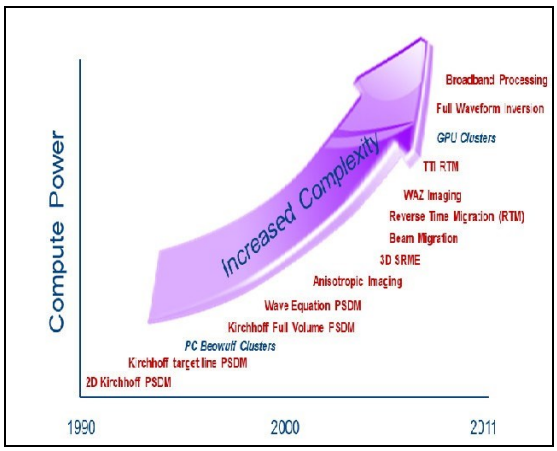

Fig 10:- Computation requirement vs Seismic Process (Courtesy IAGC)

Above graph shows that the complexity of the seismic processing has increased significantly. Previously there were only 2D processing jobs which require very less hardware resources and computing capability. Now various 3D seismic operations are in play which requires much more resources with more capability. Now let's see whether the expectations of these seismic processes are fulfilled by the processors or not.

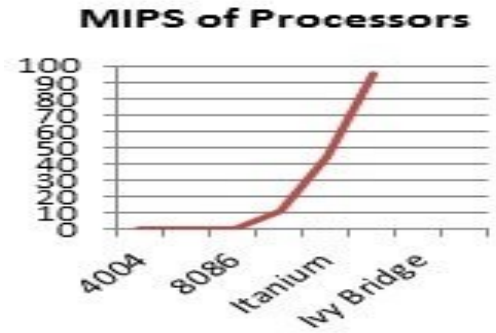

Fig 11:- Computing Capability of different Processors

As we can see, in comparison to the previous version of processors, current and expected future processors have much more computational power.

Conclusion

The fast processors developed by the IT industry will enable the advanced seismic flows requiring more computing power to be routine jobs in the seismic industry rather than testing/ experimental practice.

Current trends in the development of the technology shows that use of processors in each and every digital electronics equipment like Mobile, IPod, Tablet, and Laptop has started using high performance processor as these equipment are used as multifunction device with use of many sophisticated application. Due to these user expectations it will be a great challenge for the research and design team to reduce the manufacturing process even below 22 nm technology. It is expected that in the coming future a revolution will start in the processor technology. With smaller size, even more no of core/thread, high clock frequency etc. our computing systems will take a giant leap in the field of data processing.

Acknowledgement

This paper is a result of analysis of trends of computer processors. We are obliged to ONGC who has provided me a big platform to present myself, provided all the resources required preparing this report. We would also like to show gratitude to CGS, Dr. S. Vishwanathan, for his valuable suggestions, ideas and proper guidance which helped us preparing this report in a better way. We are also very thankful to HGS, Shri Chaman Singh, who gave me all the liberty, support and encouragement. We are thankful to Mr. Lavendra Kumar, DGM(GP) for his valuable information in context of geophysical processing. Last but not the least we are grateful to the Hardware team mate for their valuable support.

Views expressed in this paper are that of the author(s) only and may not necessarily be of ONGC.

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